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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,852	12/09/2003	Kiyonori Oyu	ELPIDA 03USFP943	5218

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EXAMINER	
NGUYEN, THINH T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 12/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/730,852	OYU ET AL.	
	Examiner	Art Unit	
	Thinh T. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *28 September 2006 and 23 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *9-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This is in response to Applicant's Amendment filed September 28th 2006 and June 23rd 2006 .

Note that the figures and reference numbers referred to in this Office Action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

2. Applicant election's of **Species I without traverse** for continuing prosecution of the case in the communication with the Office on June 23rd 2006 is acknowledged. Noted that there is a typo error in the previous Office Action since species I only have claim 1-8 and claim 9-17 has been withdrawn from consideration as being directed to non-elected invention.

3. Applicant's amendments to independent claims 1 have necessitated new grounds of rejection for claims 1-9. See MPEP § 706.07(a).

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that

the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant introduced new matter by claiming:

"Wherein **a Minimum** gate length ."-- in claim 1.

6. Claims 2-8 are rejected under 35 U.S.C. 112, first paragraph, for their dependence on claim 1.

7. The Examiner assume the applicant will correct the deficiency of claim 1 and try to examine all the claims as best as the examiner can understand.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(b/e) that form the basis for the rejections under this section made in this office action.

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claim 1,2 are rejected under 35 U.S.C. 102(b) as being anticipated by Uchida et al. (U.S. Patent 4,682,200)

REGARDING CLAIM 1

Uchida discloses (in the abstract, in column 7 lines 44-48) a semiconductor memory device comprising: a semiconductor substrate; and gate electrodes formed for a transistor on

the semiconductor substrate through a gate insulating film, wherein a gate length of the gate electrode is longer than a half pitch (or minimum processing dimension F). Noted that F is the minimum process dimension as disclosed in Kim et al. (US patent 6,501,116) column 9 lines 15-20.

REGARDING CLAIM 2

Uchida anticipates claim 2 since the channel length (the shortest distance between the drain and source diffusion region of the MOSFET) is inherently the same as the gate length as shown in the disclosure by Tobita (US patent 6,043,638)

Claim Rejections - 35 USC § 102

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(e) that form the basis for the rejections under this section made in this office action.

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claim 1-2, 3, 8, are rejected under 35 U.S.C. 102(e) as being anticipated by Furukawa et al. (U.S. Patent 6,426,175).

REGARDING CLAIM 1

Furukawa discloses (in column 16 lines 29-39) a semiconductor memory device (Furukawa discloses a DRAM or Dynamic random access memory) comprising: a semiconductor substrate; and gate electrodes formed for a transistor on the semiconductor

substrate through a gate insulating film, wherein a gate length of said gate electrode is longer than a half pitch (or minimum processing dimension F).

REGARDING CLAIM 2

Furukawa discloses (in fig 27,fig 31, the abstract) a semiconductor memory device, comprising: a first diffusion layer formed in a surface of said semiconductor substrate to function either as a source or a drain (fig 27 reference 2738,column 15 line 6); and a second diffusion layer formed in the surface of said semiconductor substrate to function either as a source or a drain, wherein the shortest distance between said first diffusion layer and said second diffusion layer is proportional to said gate length.

REGARDING CLAIM 3

Furukawa discloses (in fig 27,fig 31,fig 29, the abstract) a semiconductor memory device, wherein a gate insulating film formed (fig 29 layer 2760) on the semiconductor substrate and extending over the first diffusion layer and the second diffusion layer, wherein the gate electrode is formed on the gate insulating film.

REGARDING CLAIM 8

Furukawa discloses (in column 16 lines 29-39) a semiconductor memory device according, wherein the gate length of the gate electrode is equal to or longer than 1 .3 times the half pitch (noted that Furukawa discloses in column 16 lines 29-39 that the gate length can be 1.3 F (column 16 line 34) or 1.5F (column 16 line 32) (i.e. 1.3 or 1.5 times half pitch).

12. Claim 1-2, are rejected under 35 U.S.C. 102(e) as being anticipated by Park et al. (U.S. Patent 6,396,096).

REGARDING CLAIM 1

Park discloses (in the abstract, fig 5, column 4 lines 17-8,column 4 lines 64-67) a semiconductor memory device (Park discloses a DRAM or Dynamic random access memory) comprising: a semiconductor substrate; and gate electrodes formed for a transistor on the semiconductor substrate through a gate insulating film, wherein a gate length of said gate electrode is longer than a half pitch (or minimum processing dimension F).

REGARDING CLAIM 2

Park discloses (in the abstract, fig 5, column 4 lines 64-67,column 4 line 29) a semiconductor memory device, comprising: a first diffusion layer formed in a surface of said semiconductor substrate to function either as a source or a drain and a second diffusion layer formed in the surface of said semiconductor substrate to function either as a source or a drain, wherein the shortest distance between said first diffusion layer and said second diffusion layer is proportional to said gate length.

Claim Rejections - 35 USC § 103

13. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (U.S. Patent 6,396,096) in view of Applicant Admitted Prior Art or AAPA (Fig 2 of Applicant Application).

REGARDING CLAIM 4.

With regard to claim 4, Park discloses all the invention as set forth in the rejection of claim 2 except for going into detail about a first insulating film provided to cover the gate electrode; a first contact section formed to pass through the first insulating film to the first diffusion layer; a bit line formed on the insulating film; a second contact section formed to pass through the insulating film to the second diffusion layer, and a capacitive section formed on the first insulating film and connected to the first contact section. Applicant Admitted Prior Art, discloses a first insulating film provided to cover the gate electrode; formed to pass through the first insulating film to the first diffusion layer; a bit line formed on the insulating film; a second contact section formed to pass through the insulating film to the second diffusion layer, and a capacitive section formed on the first insulating film and connected to the first contact section.

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporated a first insulating film provided to cover the gate electrode; a first contact section formed to pass through the first insulating film to the first diffusion layer; a bit line formed on the insulating film; a second contact section formed to pass through the insulating film to the second diffusion layer, and a capacitive section formed on the first insulating film and connected to the first contact section of the AAPA into the Park et al. device since both Park and the AAPA are in the same endeavor of making DRAM.

REGARDING CLAIM 5,6

With regard to claim 5-6, as set forth in the rejection of claim 4, the combined device disclosed by the AAPA and Park disclosed all the invention except for the side length of the first contact and the second contact. These features, however, are considered obvious since it has been held that when the general condition of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

15. Claim 7 is rejected under 35 U.S.C, 103(a) as being unpatentable over Furukawa (U.S. Patent 6,426,175).

REGARDING CLAIM 7

With regard to claim 7, as set forth in the rejection of claim 1, Furukawa discloses all the invention except for the exact impurity concentration. These features, however, are considered obvious since it has been held that when the general condition of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art.

Fig. 2 PRIOR ART

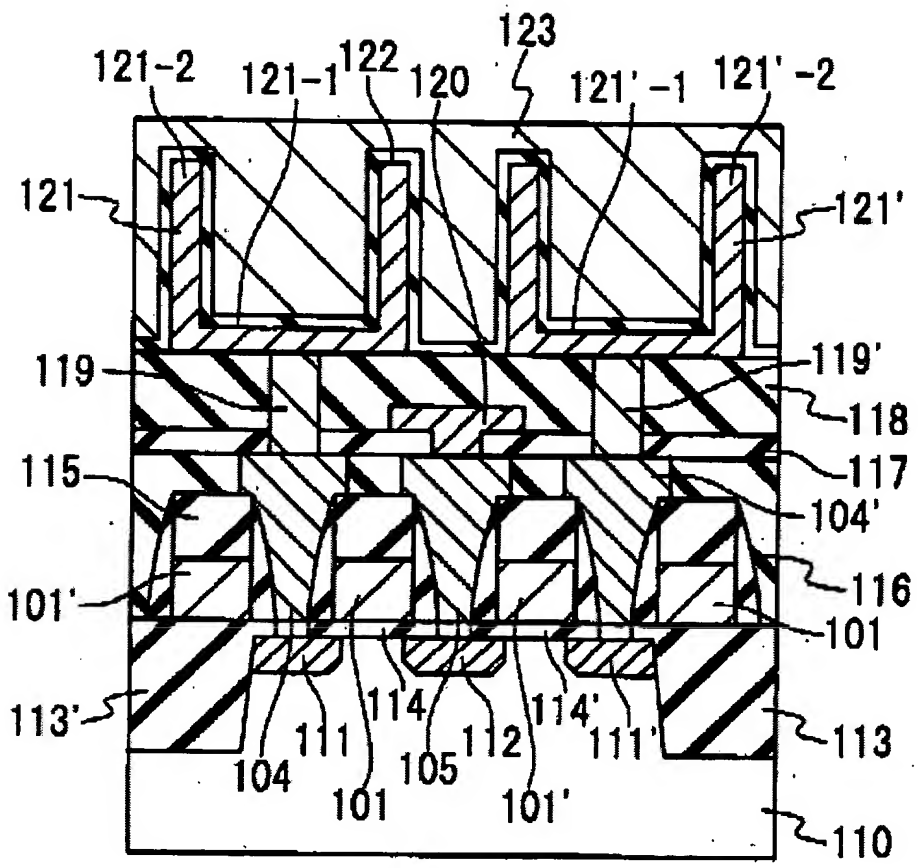
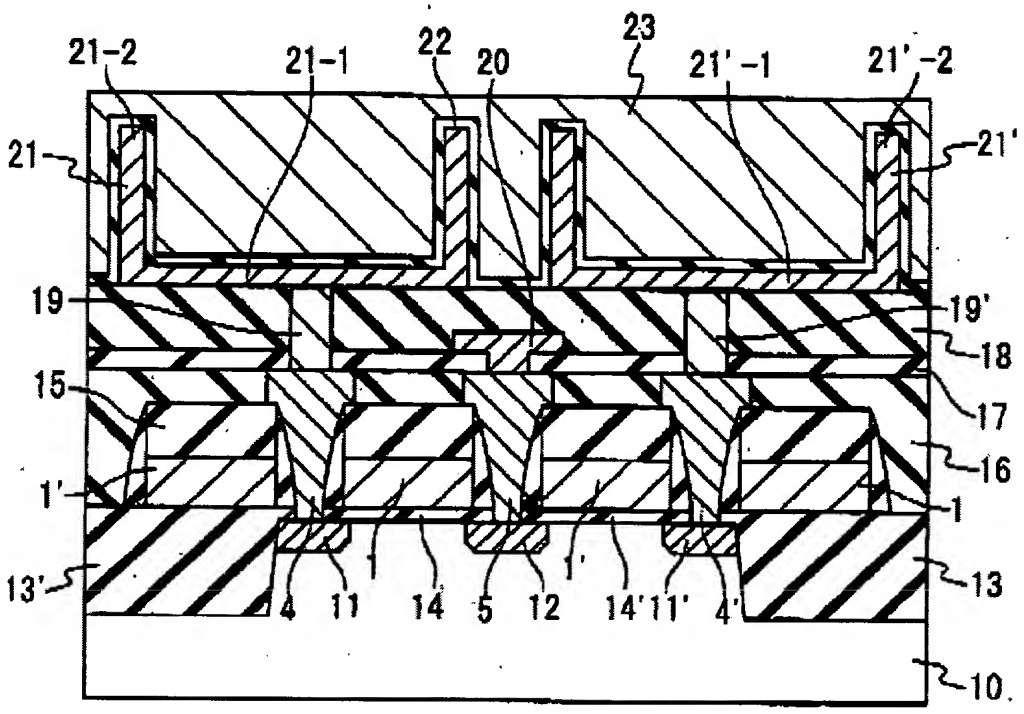


Fig. 5



APPLICANT'S INVENTION

16. applicant's arguments in the response to the Office Action rejections on June 23rd have been fully considered but they are not persuasive. The main Applicant's arguments against the three references Uchida 200 (US patent 4,682,200) , Furukawa 175 (US patent 6,426,175) and Park 096 (US patent 6,396,096) are that they does not mention half-pitch. The Examiner respectfully disagrees as the Applicant asserts in the background art (page 2 of the specification line 17-19) that in semiconductor memory -- **" a minimum processing dimension (half**

pitch) is represented by F. "--

Conclusion

18. **THIS ACTION IS MADE FINAL.** Applicant amendment to the claims necessitate new ground of rejection therefore this Action is made final. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on 9:30 am - 6:30 pm Monday to Friday..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone numbers for the organization where this application or proceeding is assigned is 571-273-8300

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thinh T Nguyen TTN

Art Unit 2818

Andy Huynh
Primary Examiner